REMARKS

Claims 1-13 and 16-18 were previously pending in this application.

Claims 1-13 and 16-18 stand rejected.

Claim 13 is rejected under 35 U.S.C 112, second paragraph.

Claims 1, 2 and 4 are rejected under 35 U.S.C. 102(b).

Claims 1, 2 and 16 are rejected under 35 U.S.C. 1002(e).

Claims 3, 5, 6-12 and 17-18 are rejected under 35. U.S.C. 103(a).

Claims 1, 3, 5, 13 and 16 are amended.

New claim 19 is added.

No new matter has been added.

Reconsideration is respectfully requested.

Claim rejections-35 USC § 112

Claim 13 is rejected under 35 U.S.C 112, second paragraph, as being indefinite for falling to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The rejection is respectfully traversed.

Claim 13 is amended to delete "the bonding wires" to correct an antecedent basis problem. Thus, the rejection is overcome. Accordingly, claim 13 is allowable.

Claim rejections-35 USC § 102

Claims 1, 2 and 4 are rejected under 35 U.S.C. 102(b) as being anticipated by applicant's admitted prior art (APA).

Claims 1, 2 and 16 are rejected under 35 U.S.C. 1002(e) as being anticipated by U.S. Patent Application Publication Pub. No. US 2002/0163055 A1 to Thomas ("Thomas").

The rejections are respectfully traversed.

Claim 1 is amended to recite:

"providing a wafer including one or more semiconductor chips, each chip comprising an active surface and a back surface, and having one or more mirrors formed on the active surface and a plurality of bond pads formed on a periphery of the chip;

forming a photoresist over the one or more mirrors;

singulating the one or more semiconductor chips from the wafer;

attaching the back surface of the one or more semiconductor chip to a top surface of a base substrate;

electrically interconnecting the bond pads of the semiconductor chip to the base substrate; and

removing the photoresist from the semiconductor chips after the electrically interconnecting the bond pads to the base substrate."

APA or Thomas does not teach or disclose the above limitations as recited in claim 1. In particular, APA does not teach or disclose, for example, "removing the photoresist from the semiconductor chips after the electrically interconnecting the bond pads to the base substrate." Also, Thomas does not teach or disclose, for example, "attaching the back surface of the one or more semiconductor chip to a top surface of a base substrate." This is because, in Thomas, the active surface, not the back surface, of the semiconductor chip 610 is attached to the base substrate 505 via solder balls. See FIG.S. 6-10 of Thomas.

Thus, APA or Thomas does not anticipate the invention recited in independent claim 1. Similarly, APA or Thomas does not teach or disclose all of the limitations recited in claim 16 and therefore does not anticipate the invention recited in independent claim 16.

As for claim 2, the Examiner states that APA teaches fully cutting the wafer (via half of the wafer fully cut). However, the differences between the half-cutting and full-cutting are well explained in the specification at page 3, lines 8-14. Even if the half of the wafer is fully cut, it does not fully cut the wafer because an additional step is required to completely cut the wafer. Thus, APA does not teach, "full-cutting the wafer," as recited in claim 2.

Thus, independent claims 1 and 16, as amended, and dependent claims 2 and 4, which depend from claim 1, is novel under 35 U.S.C. § 102 (b) or 102 (e).

Claim rejections-35 USC § 103

Claims 5, 6, 8 and 10-12 are rejected under 35. U.S.C. 103(a) as being unpatentable over APA as applied to claim 5 and furthering view of JP 356115548 to Takehara ("Takehara").

Claims 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over APA in combination with J.P 02-039442 to Mutsuo ("Matsuo").

Claim 7 is rejected under U.S.C. 103(a) as being unpatentable over APA and Takehara as applied to claim 5 and further in view of U.S. Pat. No. 5,293,511 to Poradish et al ("Poradish").

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over APA and Takehara as applied to claim 5 and further in view of JP 401053795 to Shoji ("shoji").

Claim 3, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thomas as applied to claim 1 and 16 and further in combination with Mutsuo.

The rejections are respectfully traversed.

For the reasons discussed above, APA does not teach or suggest all of the limitations of claim 5. For example, APA does not teach or suggest, "removing the photoresist from the semiconductor chips after interconnecting the electrode pads to the base substrate."

Thus, the cited references, either alone or in combination, do not teach or suggest all of the limitations of claim 5. Accordingly, the Examiner has not presented a *prima facie* case of obviousness. Consequently, the rejection of claim 5 under 35 U.S.C 103 is improper. Therefore, claim 5 is allowable and claims 6-12, which depend therefrom and recite features that are neither taught nor disclosed in the cited references, are also allowable.

Also, the rejection of claims 3, 17 and 18 is improper for the reasons discussed above. Thus, claims 3, 17 and 18, which depend from allowable claims 1 and 16, respectively, are allowable.

For the foregoing reasons, reconsideration and allowance of claims 1-13 and 16-18 of the application as amended is solicited. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION

Please replace the paragraph beginning at page 2, lines 24-25 with the following:

[In] The [wafer-breaking step,] silicon particles [scraps are]generated during the wafer-breaking step are then [. Therefore, the silicon particles are]removed (step 76).

Please replace the paragraph beginning at page 6, line 22-26, with the following:

As shown in FIGS. 6 through 8, the manufacturing process starts with preparing the wafer 110 (step 191). The silicon wafer 110 comprises a plurality of mirror-driving integrated circuits (not shown) formed by conventional techniques. A plurality of semiconductor chips 112 [is]are formed on the wafer 110. Scribe lines 118 are also formed between the neighboring semiconductor chips 112, where the circuits are not formed.

IN THE CLAIMS

1. (Twice amended) A method for manufacturing a semiconductor package, said method comprising:

providing a wafer including one or more semiconductor chips, each chip comprising an active surface and a back surface, and having one or more mirrors formed [thereon] on the active surface and a plurality of bond pads formed on a periphery of the chip;

forming a photoresist over the one or more mirrors;

singulating the one or more semiconductor chips from the wafer;

[mounting] attaching the back surface of the one [ore] or more semiconductor chip [on] to a top surface of a base substrate;

electrically interconnecting the bond pads of the semiconductor chip to the base substrate; and

removing the photoresist from the semiconductor chips after the electrically interconnecting the bond pads to the base substrate.

3. (Once amended) The method of claim 1, after said forming the photoresist, further comprising:

forming a metallic layer over a back surface of the wafer,

wherein said [mounting] attaching is performed using a metallic adhesive.

5. (Once amended) A method for manufacturing digital micro-mirror device (DMD) packages, said method comprising:

providing a wafer including a plurality of DMD semiconductor chips, each chip comprising an active surface and a back surface and having one or more mirrors formed on substantially the center of [an] the active surface of the chip, a plurality of electrode pads formed on the periphery of the active surface;

forming a photoresist over the mirrors;

forming a metallic layer on a back surface of the wafer;

separating the wafer into the individual semiconductor chips;

[mounting] attaching the back surface of each semiconductor chip [on] to an upper surface of a base substrate using a metallic adhesive;

interconnecting the electrode pads of the semiconductor chip to the base substrate with one or more bonding wires;

removing the photoresist from the semiconductor chips after interconnecting the electrode pads to the base substrate;

forming an anti-sticking film on the active surface of the semiconductor chip for protecting the semiconductor chips from dust and moisture; and

hermetically sealing the semiconductor chip and the bonding wires on the upper surface of the base substrate.

13. (Once amended) The method of claim 1, wherein said hermetically sealing the semiconductor chip [and the bonding wires] is performed at a predetermined temperature, said predetermined temperature being not higher than the temperature on which said attaching the semiconductor chip to the base substrate is performed.

16. (Once amended) A method for manufacturing a semiconductor package, said method comprising:

providing a wafer including one or more semiconductor chips, each chip comprising an active surface and a back surface and having one or more mirrors and electrodes formed [thereon] on the active surface;

coating the one or more mirrors with a photoresist film;

singulating the one or more semiconductor chips from the wafer;

[mounting] attaching the back surface of the one [ore] or more semiconductor chip [on] to a top surface of a base substrate using a metallic adhesive;

electrically interconnecting the electrodes of the semiconductor chip to the base substrate; and

removing the coated photoresist film from the one or more mirrors of the semiconductor chips after the interconnection.

Claim 19 is new.